EE140 Design Project

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1 Overview

1.1 Topology

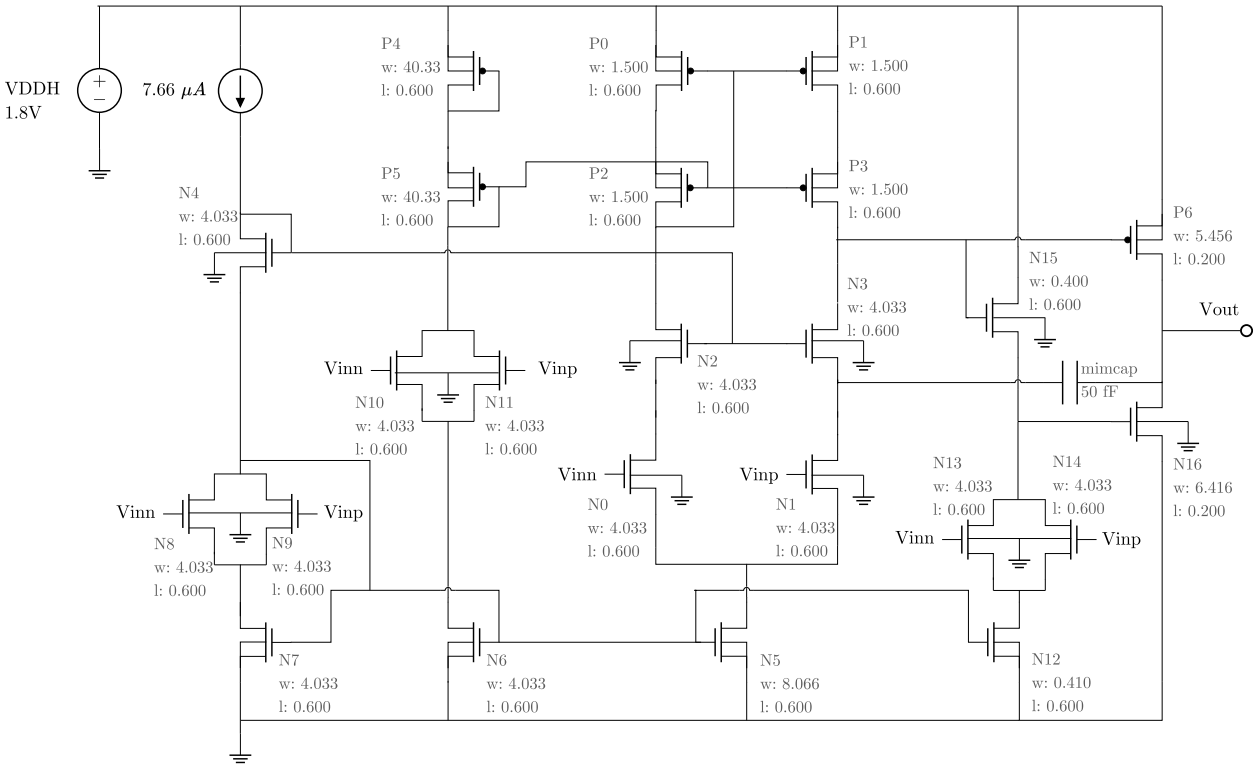


Figure 1: Full Circuit Schematic. All dimensions are in μm and all devices are 2V.

I designed the following two stage amplifier composed of a telescopic differential first stage and a Class AB common source second stage.

- **Stage 1: Telescopic Differential** to achieve high gain through a large R_{OUT} and ensure minimum static error. This uses VDDH to ensure all transistors have enough headroom to remain in saturation.

  In the main telescopic stack, all NMOS devices are sized identically and all PMOS devices are sized identically. Both device types share the same length to be consistent.

  Two distinct gate voltages in the telescopic stack are biased by individual branches which see mirrored current.

- **Stage 2: Class AB Common Source** to achieve 1.4V output swing with minimum slewing. This also uses VDDH as VDDL cannot support 1.4V swing.

  The top PMOS $P6$ is biased directly by Stage 1 while a source follower NMOS offsets this voltage to bias the NMOS $N16$.

1.2 Specification Comparison

Table 1: Specification Comparison Table

Parameter	**EE 140 / EE 240A**	**My Design**
Technology	gpdk045	gpdk045
Power Supplies	GND (0V), VDDL ($\leq 1.1V$) VDDH ($\leq 1.8V$)	GND (0V), VDDH (1.8V)
Closed Loop DC Gain	2	2
Load	150 Ω, 60pF	150 Ω, 60pF
Settling Time	180 ns	119.8 ns
Total Error	$\leq 0.2\%$	$\leq 0.2\%$
Output Voltage Swing	$\geq 1.4V$	$\geq 1.4V$
Max Current Mirror Ratio	10	9.84
Max Total Capacitance	10pF / 5pF	50 fF
Max Total Resistance	200 kΩ / 100 kΩ	0 Ω
CMRR at DC	≥ 65 dB	91.47 dB
PSRR at DC	≥ 50 dB	61.61 dB (VDDH)
Phase Margin	$\geq 45°$	66.65°
Power Consumption	≤ 2.75 mW / ≤ 1.5 mW	212.4 μW

2 Design

2.1 Calculating Gain and Settling Time Bounds

I first calculated the β factor and minimum open loop gain. I evenly split the error bound of 2% between ε_s and ε_d to start, so I set $\varepsilon_d = 0.001$.

$$\beta = \frac{C_F}{C_F + C_S} = \frac{1}{3} \qquad \varepsilon_s = \frac{1}{1 + \beta A_{OL}} \implies A_{OL\_min} = \frac{1 - \varepsilon_s}{\beta \varepsilon_s} = 2997$$

Thus, the minimum open loop gain the amplifier requires is 2997 V/V. I then calculated minimum settling time considering the display size and refresh rate.

$$t_s = \frac{1}{(\text{Refresh Rate})(\text{Display Size})} = \frac{1}{(60)(272)(340)} = 180 \text{ ns}$$

2.2 Calculating Ideal Small Signal Parameters

Following the guideline suggestions, I modeled my two stage amplifier using ideal voltage-driven current sources and output resistances. These have transconductance and resistance values of $\mathbf{g_{m1}}, \mathbf{g_{m2}}, \mathbf{R_1}, \mathbf{R_2}$.

I approximated the following expressions for pole locations and the open loop transfer function.

$$\text{Dominant Pole} \approx \frac{1}{R_1 C_{c\_Miller}} \approx \frac{1}{R_1 g_{m2} R_2 C_c} \qquad \text{Second Pole} \approx \frac{1}{(\frac{1}{g_{m2}} || R_2) C_L} \approx \frac{g_{m2}}{C_L}$$

$$\text{LG(s)} = \beta A_{OL}(s) = (\frac{1}{3})(\frac{g_{m1} R_1 g_{m2} R_2}{(1 + s * R_1 g_{m1} R_2 C_c)(1 + s * \frac{g_{m1}}{C_L})}) \approx \frac{\frac{1}{3} g_{m1} R_1 g_{m2} R_2}{(1 + s * R_1 g_{m1} R_2 C_c)} \approx \frac{g_{m1}}{3 s C_c}$$

Above, I made the approximation that the loop gain transfer function is dictated by the dominant pole. I found that it reaches unity gain at $w_{u,LG} \approx \frac{g_{m1}}{3C_c}$

Supposing $V_{out}(t) = A_0(1 - e^{-w_{p,CL}t})$ where $w_{p,CL}$ is the closed loop 3dB frequency, I found the 3dB frequency. I used my chosen value for ε_d which I know is true at minimum settling time t_s.

$$\varepsilon_d(t_s) = \frac{V_{out}(\infty) - V_{out}(t_s)}{V_{out}(\infty)} = e^{-(w_{p,CL})t_s} = 0.001 \implies w_{p,CL} \approx 35 \text{ M}\frac{rad}{s} \approx 6.1 \text{ MHz}$$

Using the fact that $w_{p,CL} = w_{u,LG}$ I found that $\mathbf{g_{m1}} = \mathbf{115}\mu\mathbf{s}$. Aiming for 75° phase margin, I know that $75° = 180° - 90° - \arctan(\frac{w_{u,LG}}{\frac{g_{m2}}{C_L}})$ where $\frac{g_{m2}}{C_L}$ is the second pole. I found that $\mathbf{g_{m2}} = \mathbf{8.58\ mS}$.

Using the loop gain expression $\beta A_{OL} = \beta g_{m1} R_1 g_{m2} R_2 = \beta(115\mu s) R_1 (8.58ms) R_2$, I found that I need $\mathbf{R_1 R_2} = \mathbf{3\ G\Omega}$.

2.3 Topology and Scripting: Stage 1

I proceeded with a telescopic first stage due to its high gain, aiming for $R_1 \approx 2M\Omega - 20M\Omega$ to take the majority if not all of $R_1 R_2 = 3\ G\Omega$. I wrote a python script that follows the below process to size the first stage transistors.

1. I chose to set $\frac{\mathbf{g_m}}{\mathbf{I_D}} = \mathbf{15}$ (a balance between efficiency and ensuring strong inversion) and used this to find $V_{GS,n}$ and $V_{SG,p}$ from the LUTs.

2. Assuming mid-rail first stage output and that voltage is equally dropped across each transistor, I found $V_{DS,n}$. I approximated that $V_{SG,p}$ is equally dropped across each PMOS in the mirror. This yielded $V_{SD,p}$

3. Using $\frac{g_m}{I_D}$, $V_{DS,n}$ (or $V_{SD,p}$), and variable Length L, I found $r_{o,n}$, $r_{o,p}$, and f_T in terms of L.

4. I created an expression for R_{out} and sweeped R_{out} and f_T over L. I chose the largest L that satisfied $f_T \geq 10 f_u$ to maximize R_{out} and thus the gain of Stage 1. I used this $\mathbf{L = 0.60\ \mu m}$ and my ideal $\mathbf{g_{m1}}$ to find $\mathbf{I_D}$ and thus $\mathbf{W_p = 2.05\ \mu m}$ and $\mathbf{W_n = 4.033\ \mu m}$ using $\frac{I_D}{W}$.

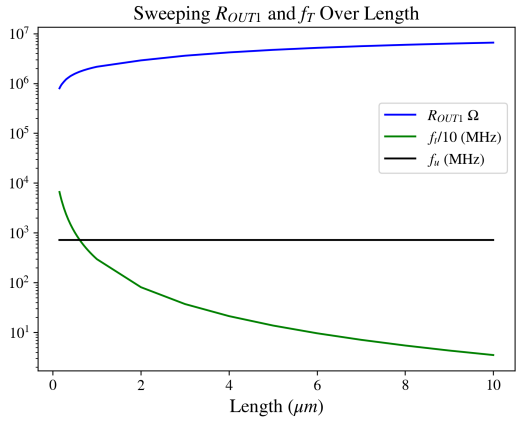


Figure 2: LUT Sweep Over L

2.4 Current Mirrors and Biasing Stage 1

I use a single 7.66 μA current source. This is the nominal I_D my transistors are sized for. This current is mirrored 1:1 to each of two biasing branches and doubled to generate the telescopic tail current.

Replica Biasing:

I had noticeable mismatch in my current mirror due to the input pair applying a common mode offset to the tail transistor's drain node.

Two dummy transistors are placed above each current mirroring transistor to mimic the input pair and apply the same voltage offset. This keeps V_{DS} identical and improves current matching.

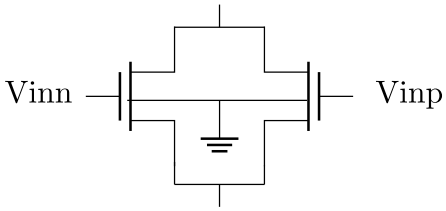


Figure 3: NMOS Biasing

Biasing NMOS Gate:

Assuming minimum ΔV drop across each transistor, starting at GND, $(\Delta V_{N5} + \Delta V_{N0,1} + V_{GS\_N2,3}) = (3\Delta V_n + V_{TH,n})$ is gained across the tail current transistor, input NMOS devices, and V_{GS} of the cascode NMOS devices before reaching their gate.

On the biasing branch, the current mirror and input pair replica account for $2\Delta V$. An identical NMOS produces the remaining $\Delta V + V_{TH}$ and is diode connected to ensure it is in saturation.

Biasing PMOS Gate:

Again assuming minimum ΔV drop, $V_{SG\_P0} = (\Delta V_P - |V_{TH,p}|)$ is dropped across the wide-swing mirror. ΔV_{P2} is gained across $P2$ and V_{SG_P2} is dropped to arrive at a gate voltage of $(3\Delta V_p + V_{TH,p})$.

This bias is achieved by dropping $\frac{1}{2}\Delta V + |V_{TH,p}|$ across each of two diode-connected PMOS devices, whose widths are multiplied by 4 to achieve $\frac{1}{2}\Delta V$. Note that I adjusted the widths later (see Post-Simulation Iteration section).

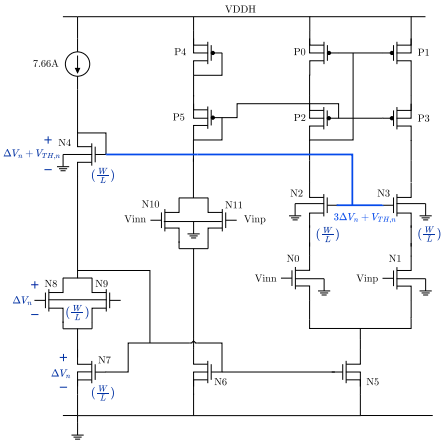


Figure 4: NMOS Biasing

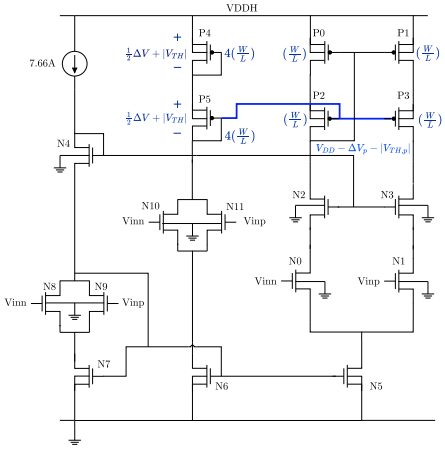


Figure 5: PMOS Biasing

2.5 Topology and Scripting: Stage 2

When designing my Class AB second stage, I prioritized minimizing slew and ensuring high output swing. I wrote a python script to do the following:

1. Identify peak current draw as $I_{PEAK} = C_L \frac{1.4V \text{ swing}}{t_s} = 466\mu A$ where t_s is maximum settling time.

2. I approximated Stage 2 gain to equal 10 $\frac{V}{V}$ and thus max input swing is 140 mV. Knowing nominal $V_{SG,P6}$ of the PMOS to be $V_{DD} - V_{OUT\_STAGE1}$, I now knew maximum $V_{SG,P6}$.

3. I chose a Length $\mathbf{L = 0.2\ \mu m}$ and calculated $\frac{I_D}{W}$ at which this maximum V_{SG} is achieved. I found Width as $\mathbf{W_{N16} = I_{PEAK} * \frac{I_D}{W} = 27.28\ \mu m}$.

4. I chose $\frac{g_m}{I_D} = 16$ for the output NMOS (a balance between low ΔV and ensuring the transistor is in saturation), sized it to the same length and nominal I_D flowing through the PMOS, and found Width $\mathbf{W_{P6} = 58.33\ \mu m}$.

Source Follower Sizing:

Knowing that $V_{GS,N15}$ of the NMOS source follower must equal ($V_{OUT\_STAGE1} - V_{GS,N16}$), I found the needed $V_{GS,N15}$ and adjusted the transistor's width and current mirror until this was achieved.

Compensation Capacitor:

I first implemented my compensation capacitor between V_{OUT_STAGE1} and V_{OUT_STAGE2}, but my amplifier remained on the edge of meeting the settling time specification. I switched to using Ahuja compensation and connected C_c to the node beneath my telescopic NMOS instead. This lowered settling time significantly.

2.6 Post-Simulation Iteration

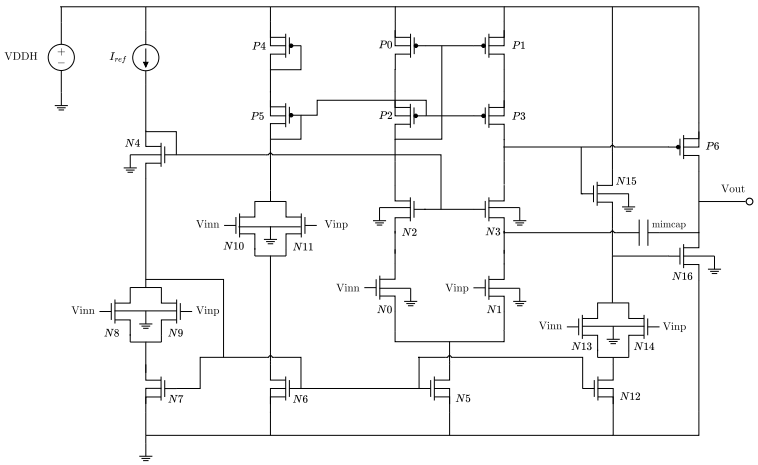
I observed that the NMOS devices in my telescopic stage were being pushed into triode and increased the width of by PMOS gate bias-setting transistors to push that gate and thus the headroom of the NMOS devices up.

I then saw my Stage 2 PMOS $P6$ was in triode, and lowered the width of the telescopic PMOS devices to push down V_{OUT_STAGE1} and increase $V_{GS,P6}$. I acknowledge that I could have instead decreased width of the bias-setting transistors slightly.

My Stage 2 PMOS was pushing less current that the NMOS pulled so I adjusted that output NMOS $N16$'s width until both devices saw identical I_D. These changes are elaborated on in the Discussion section.

I also adjusted the source follower as needed to maintain desired $V_{GS,N16}$. Throughout all the above changes I remained conservative whenever making changes that would increase nominal current and made alternative choices when possible to keep power low. I also ensured all devices remained in saturation.

3 Transistor and Bias Summary



Transistor	**W** (µm)	**L** (µm)	I_d (µA)	V_{gs} (m**V**)	G_m (µS)	g_{ds} (µS)
Telescopic First Stage						
N0	4.033	0.600	7.153	550.1	110.4	3.901
N1	4.033	0.600	7.153	550.1	110.4	3.901
N2	4.033	0.600	7.153	594.6	112.0	2.021
N3	4.033	0.600	7.153	594.6	112.0	2.022
P0	1.500	0.600	7.153	600.1	77.23	3.845
P1	1.500	0.600	7.153	598.0	78.70	3.844
P2	1.500	0.600	7.153	600.1	77.23	2.841
P3	1.500	0.600	7.153	598.0	78.70	2.837
Telescopic Biasing and Mirrors						
N4	4.033	0.600	7.665	599.5	118.0	2.366
N5	8.066	0.600	14.31	543.7	215.2	18.85
N6	4.033	0.600	7.729	543.7	115.3	7.716
N7	4.033	0.600	7.665	543.7	114.4	7.978
N8	4.033	0.600	3.833	518.1	67.57	2.536
N9	4.033	0.600	3.833	518.1	67.57	2.536
N10	4.033	0.600	3.864	509.9	68.17	2.536
N11	4.033	0.600	3.864	509.9	68.17	1.260
P4	40.33	0.600	7.728	436.3	199.0	3.783
P5	40.33	0.600	7.728	436.3	199.0	3.783
Class AB Output Stage						
N12	0.410	0.600	1.295	543.7	16.93	0.940
N13	4.033	0.600	0.648	440.9	14.64	0.546
N14	4.033	0.600	0.648	440.9	14.64	0.546
N15	0.400	0.600	1.295	594.6	17.57	0.170
N16	6.416	0.200	52.53	604.9	685.0	17.65
P6	5.456	0.200	52.75	600.4	664.4	15.90

4 Discussion

4.1 AC Simulation

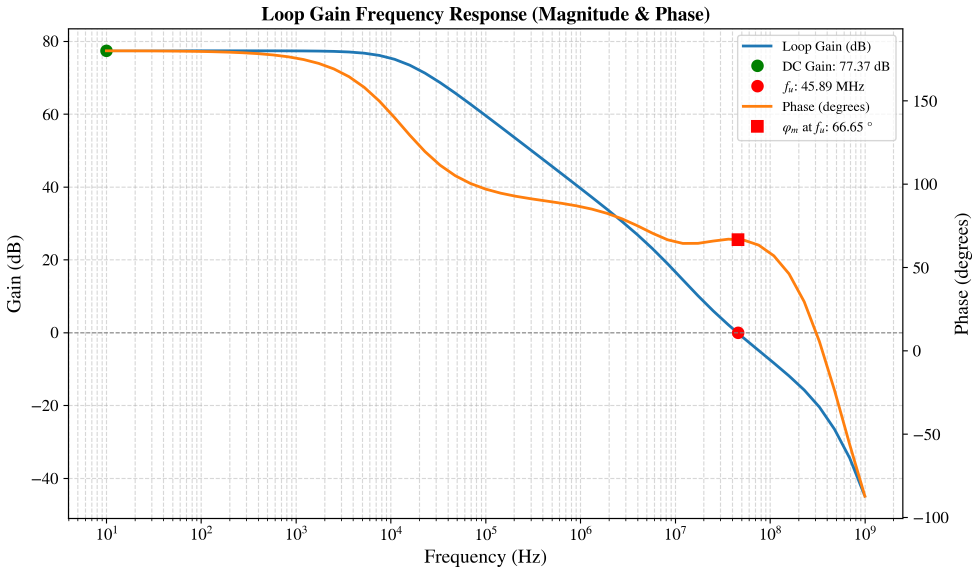


Figure 6

My amplifier has a high DC Loop Gain of 77.37 dB, created primarily by the high R_{OUT} of the telescopic first stage. This high gain ensures that static gain error is kept to a minimum and the closed loop gain is close to 2.

My phase margin is 66.65°. I originally started with a 1pF C_c and larger phase margin. I lowered C_c to bring down phase margin, decreasing settling time dramatically by allowing the output to fall within the error window faster.

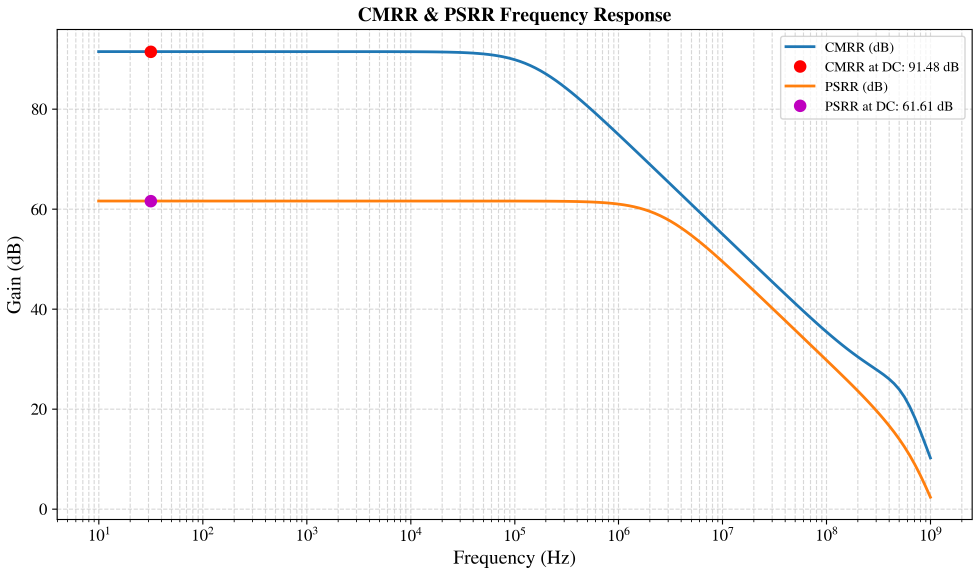


Figure 7

My circuit has a high DC CMRR of 91.48 dB and a DC PSRR of 61.61 dB. Note that the plot above displays PSRR for VDDH, as I do not use VDDL. My topology achieved this CMRR and PSRR without the need for iterative changes from my script. Prior to the PSRR specification being relaxed, I attempted to increase PSRR by raising the length of my devices to increase r_o and grow input-output gain relative to supply-output gain. I undid these changes as they affected other parts of my circuit.

4.2 Transient Simulation

4.2.1 Overview and Output at C_L

Test	Output	Spec	Weight	Pass/Fail	Min	Max	5mV	350mV
Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter	Filter
project_lib_tb_tr...	vout							
project_lib_tb_tr...	vout_load							
project_lib_tb_tr...	vout_stage1						eval err	eval err
project_lib_tb_tr...	i_vddl							
project_lib_tb_tr...	i_vddh							
project_lib_tb_tr...	avg_pow_vddl				0	0	-0	-0
project_lib_tb_tr...	avg_pow_vddh				150.7u	212.4u	150.7u	212.4u
project_lib_tb_tr...	avg_pow_tot				150.7u	212.4u	150.7u	212.4u
project_lib_tb_tr...	mid_vout				900m	900m	900m	900m
project_lib_tb_tr...	err_high							
project_lib_tb_tr...	rise_time				40.46n	119.8n	40.46n	119.8n
project_lib_tb_tr...	err_low							
project_lib_tb_tr...	fall_time				43.65n	119.8n	43.65n	119.8n
project_lib_tb_tr...	settle_time				43.65n	119.8n	43.65n	119.8n

Figure 8

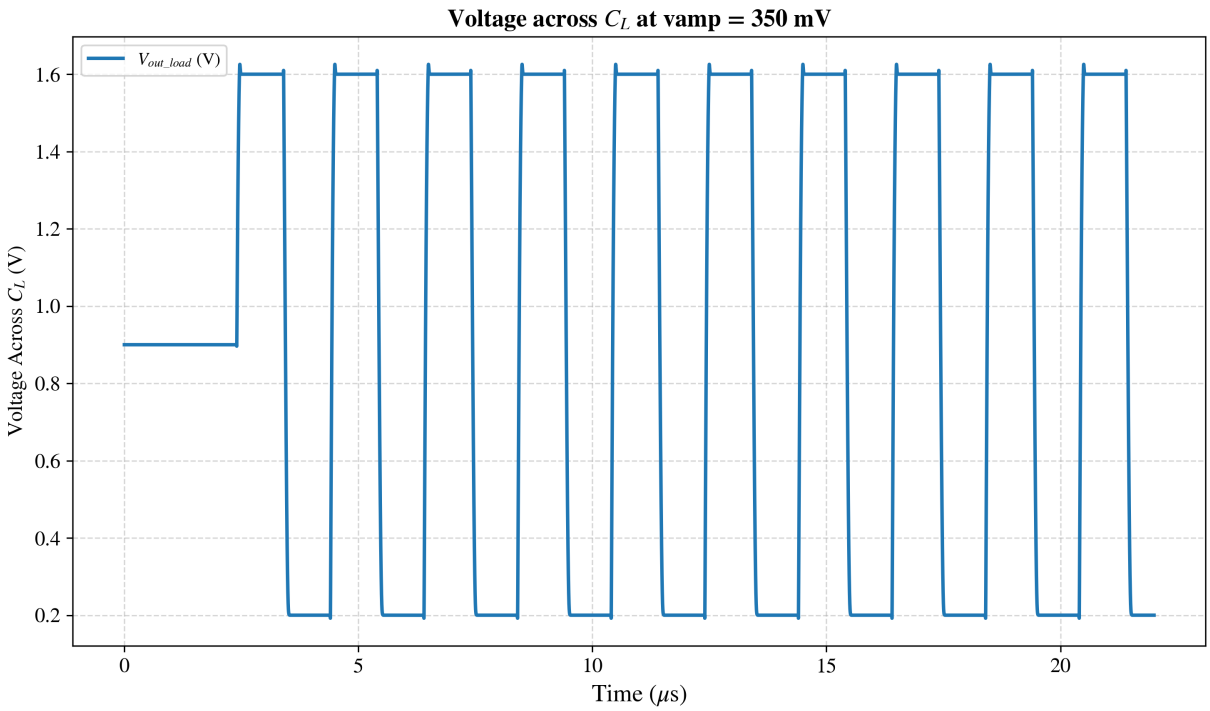


Figure 9

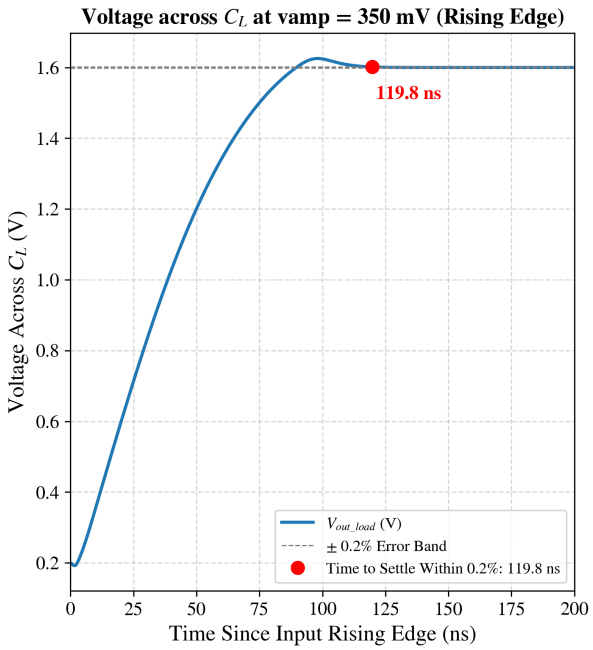


Figure 10

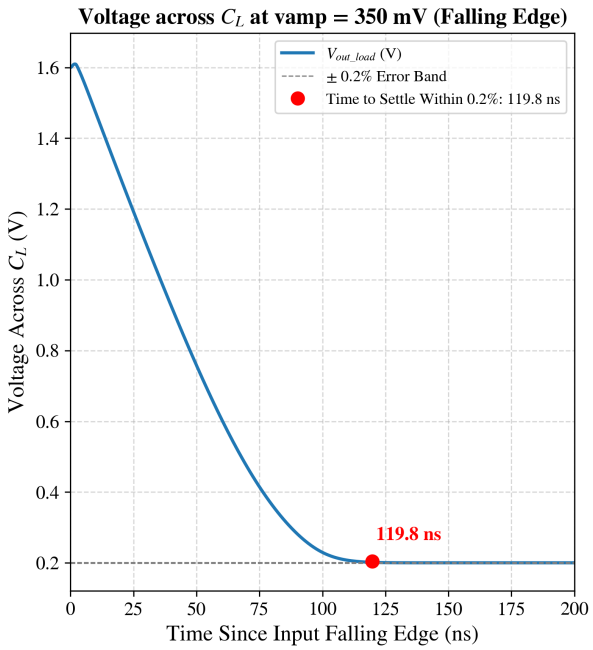


Figure 11

Figures 9-11 display the output voltage at the load capacitor for a input signal of amplitude 350 mV. The output reaches the desired target well within the minimum settling time. I sized

the Class AB second stage to support peak required current and adjusted the compensation capacitor to ensure that the combined effects of slew and linear settling are not significant enough to push settling time beyond 180 nS.

There is also an observable dip and spike in the output waveform before the signal rises and falls, respectively. This is likely due to the RHP zero created by the compensation capacitor.

I did not add a compensation resistor as the effects of this pole were not significant enough to require it.

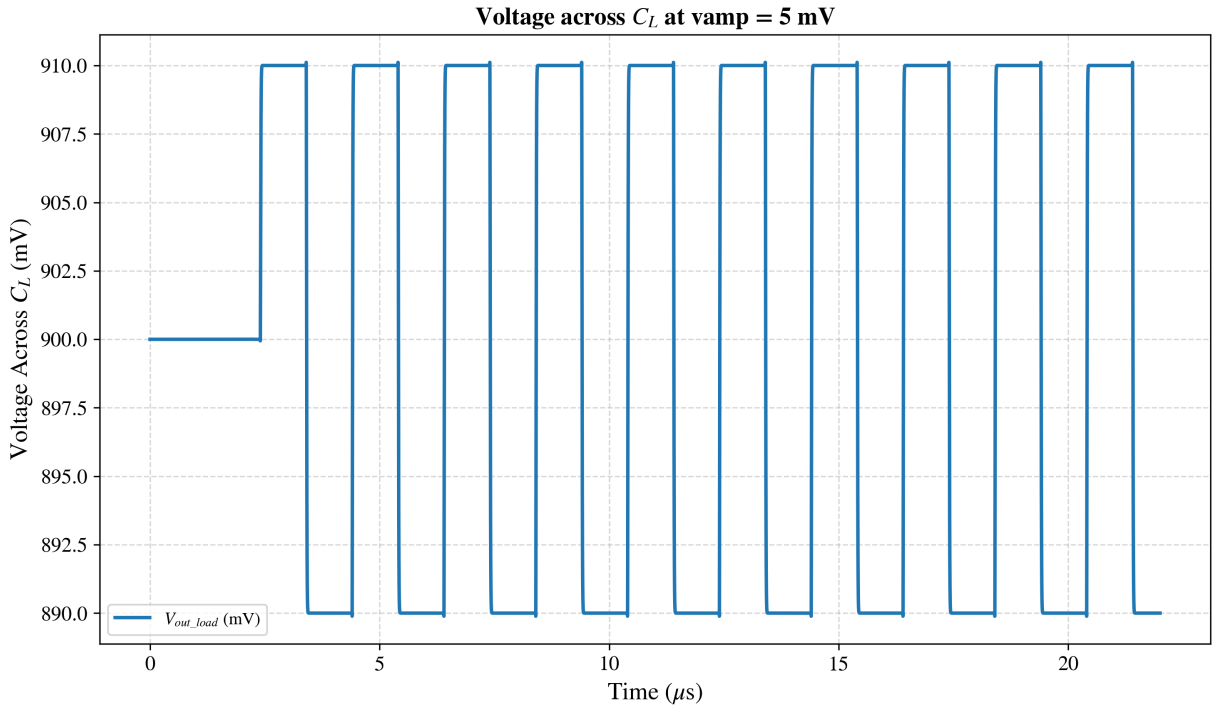


Figure 12

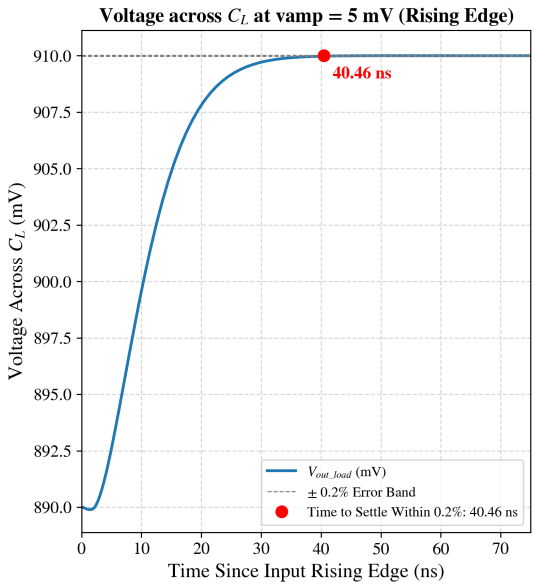


Figure 13

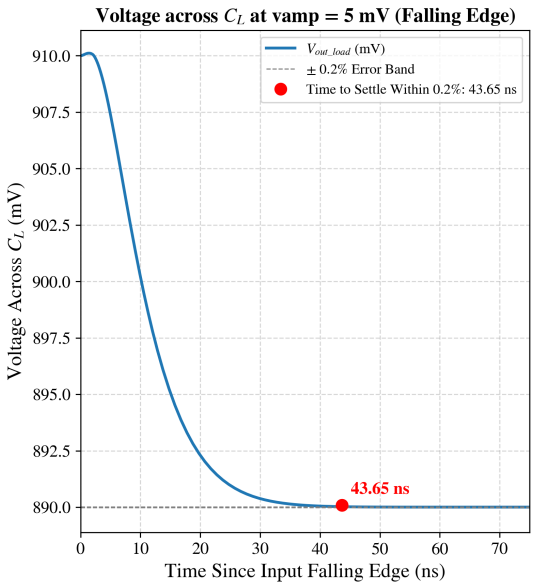


Figure 14

The amplifier behaves similarly to the 5 mV input as it did to the 350 mV input. There is minimal slew and even less linear settling seen at the output. This makes sense for a smaller input step.

4.2.2 Settling Error

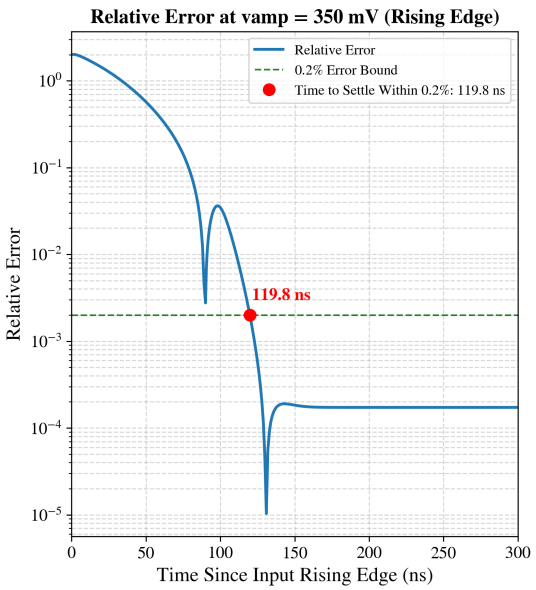


Figure 15

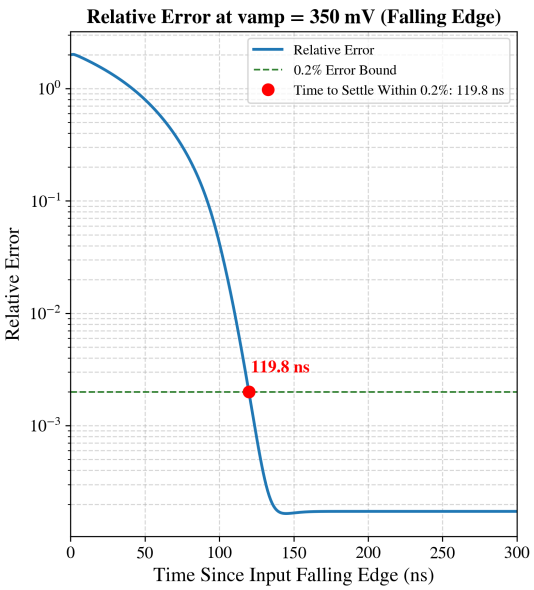


Figure 16

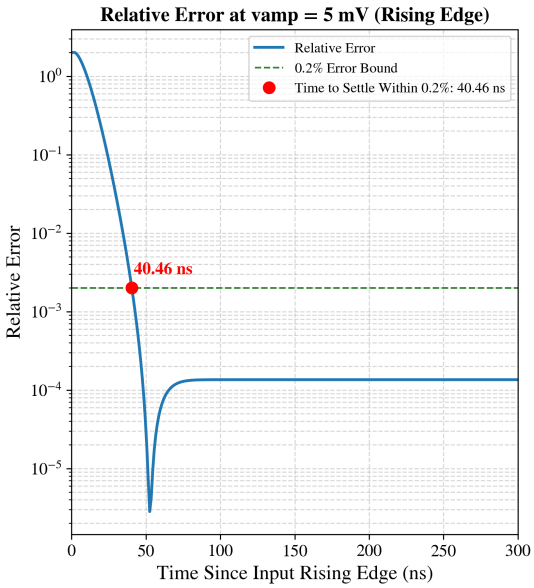


Figure 17

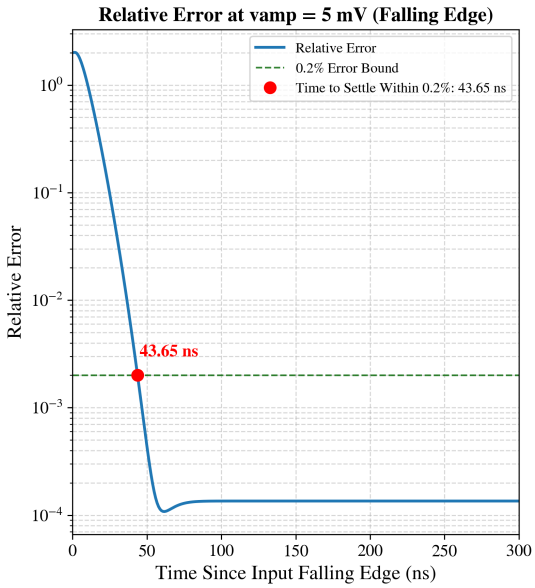


Figure 18

Figures 15-18 display settling error when the amplifier sees 5 mV and 350 mV inputs. This is defined as the ratio $\frac{|\text{Target Output - Actual Output}|}{\text{Input Step Size}}$.

By adjusting the compensation capacitor to decrease phase margin, I allow the output to oscillate longer but the final oscillations remain below the allowable error window. This is more noticeable on the rising edges.

4.2.3 Amplifier Output Before R_L

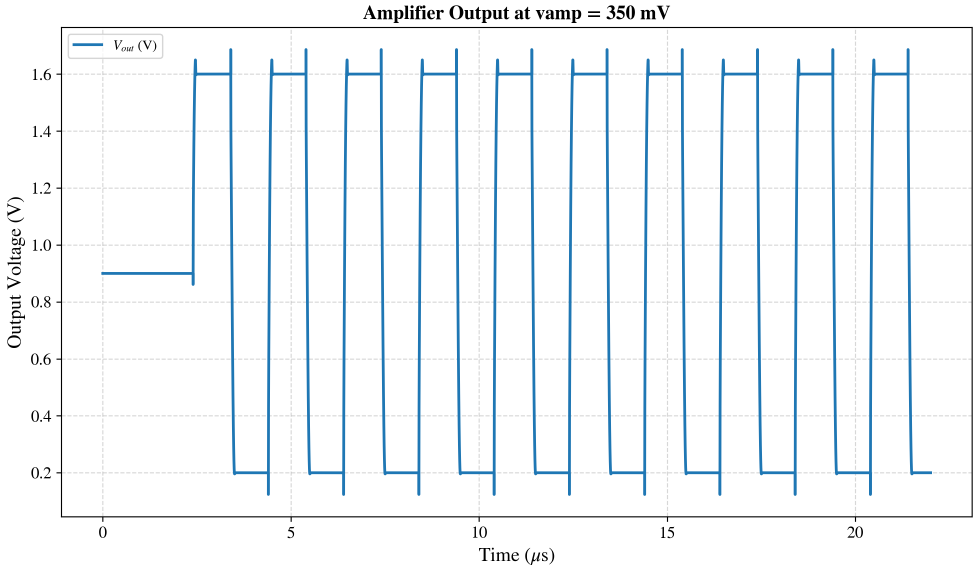


Figure 19

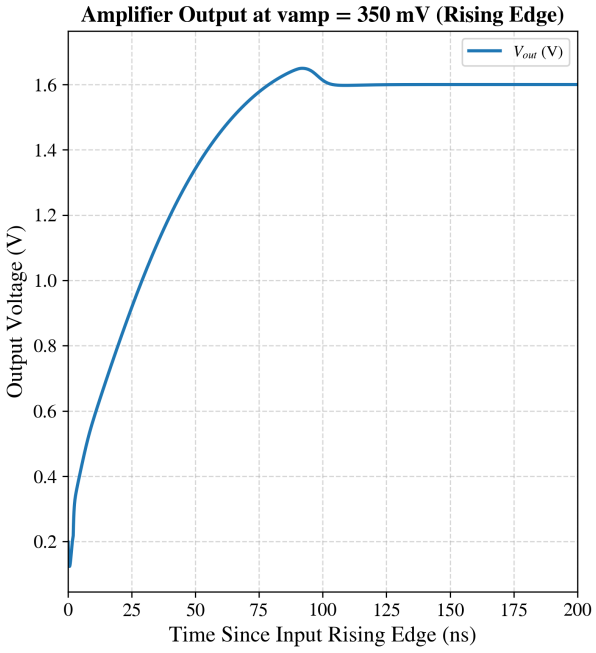


Figure 20

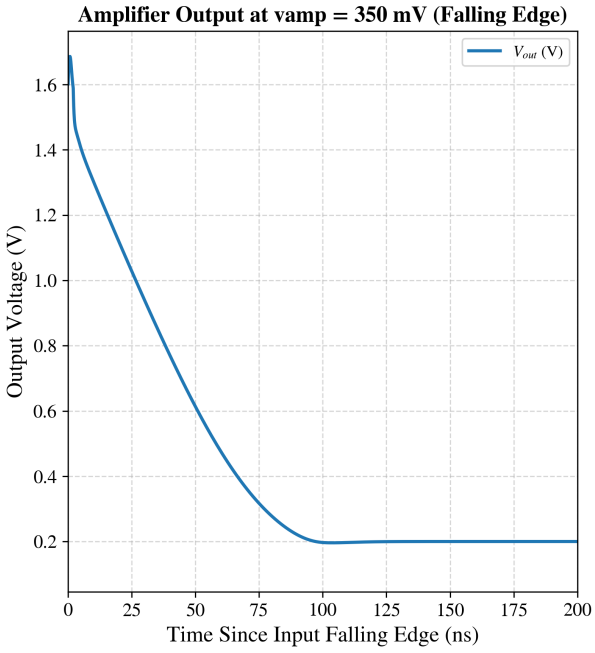


Figure 21

Figures 19-21 display the amplifier output before the load resistor. Here, the settling error is slightly greater, and there is a larger spike before the output settles, particularly on the rising edges. This may be because the the waveform at C_L is smoothed out by the low-pass

filter formed by R_L and C_L.

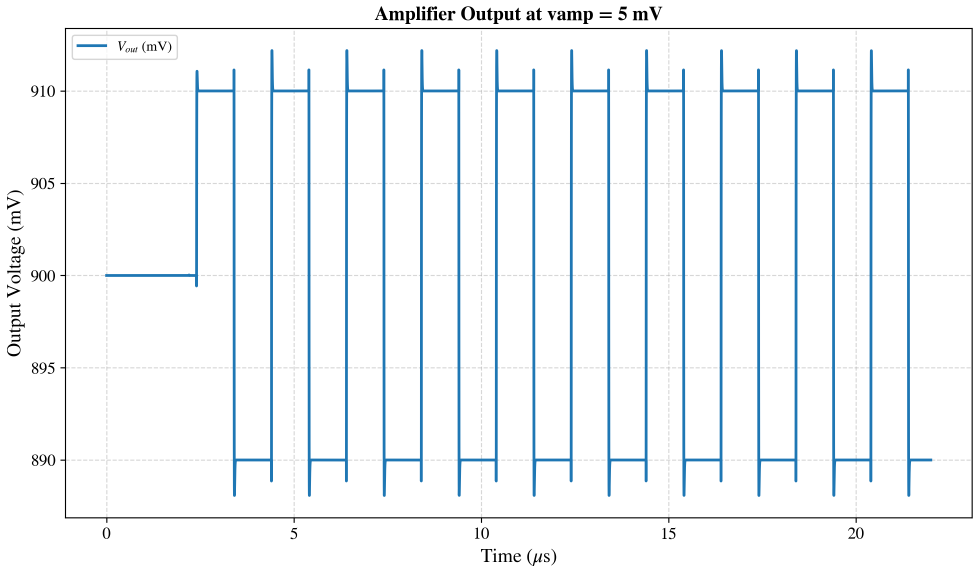


Figure 22

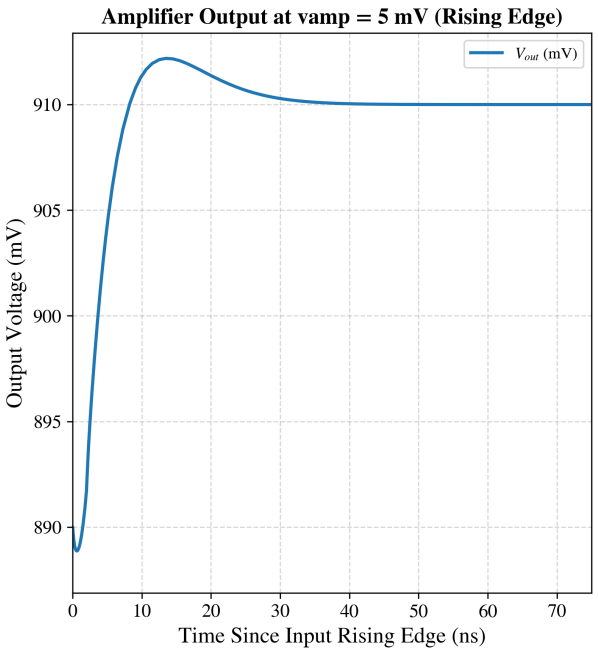


Figure 23

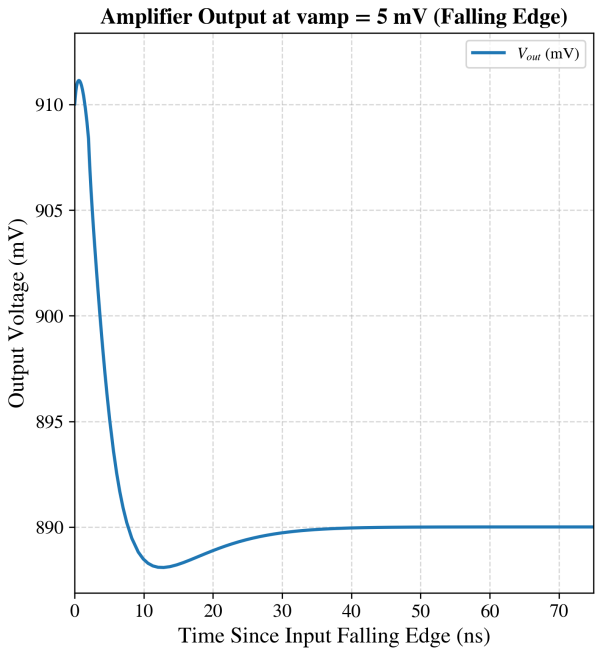


Figure 24

Figures 22-24 display the same raw amplifier output for a 5 mV input. The output waveform behavior compares to the waveform with a 350 mV input. As expected, the error appears lower than in the 350 mV case.

4.2.4 Current Draw

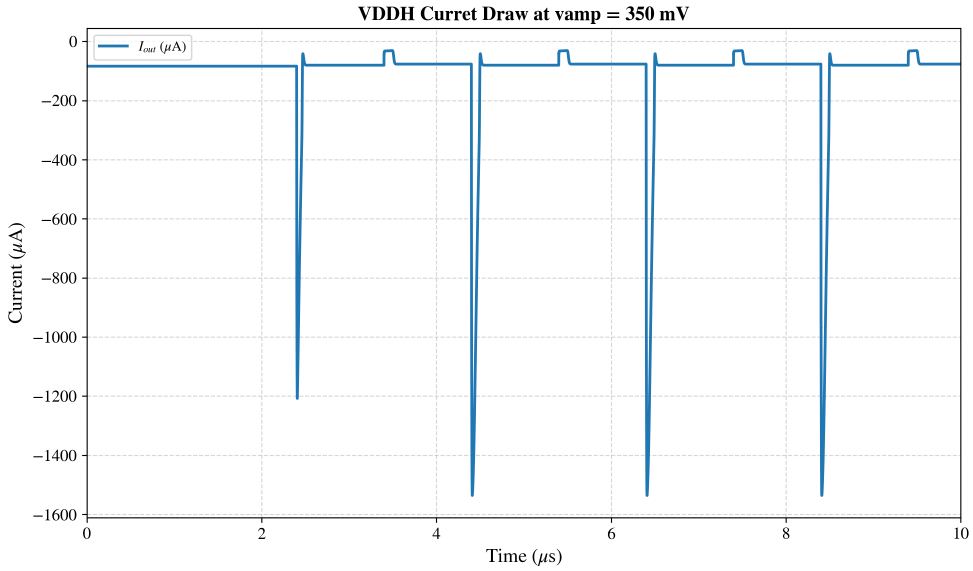


Figure 25

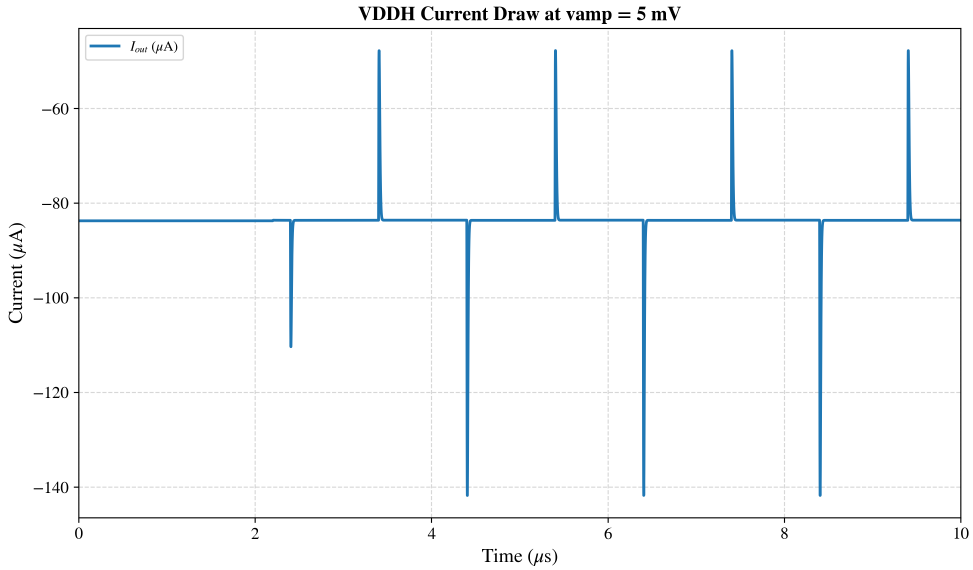


Figure 26

Figures 25 and 26 display current draw from VDDH for 350 mV and 5 mV inputs. I only plot VDDH current draw as I did not use VDDL. There are clear spikes during the rising and falling edges when current draw peaks. I designed my Class AB stage to support this peak current with minimum slewing, while nominal current draw is minimized.

After sizing my Class AB output transistors to meet peak current draw, I lowered the width of the PMOS $P6$ and NMOS $N16$ by equal amounts to lower their nominal I_D from roughly 200 μA to 51 μA.

For the 350 mV input, there is significantly higher current draw on the rising edges than the falling edges. This implies mismatch between the Class AB output stage PMOS and NMOS. While I matched nominal I_D between the two transistors, I could iterate further on transistor sizing or alter my scripting methodology to ensure they behave identically during the amplifier's full operating region.

4.3 Test-Benches

I did not alter the topology of the testbenches from what staff provided. I used the following input and output bias voltages:

$$\mathbf{V_{ICM} = 0.7\ V} \qquad\qquad \mathbf{V_{OCM} = 0.9\ V}$$

I estimated V_{ICM} using the V_{GS} values predicted by my script and iteratively tuned it after running simulations. I kept $V_{OCM} = 0.9V$ to bias the output at mid-rail.

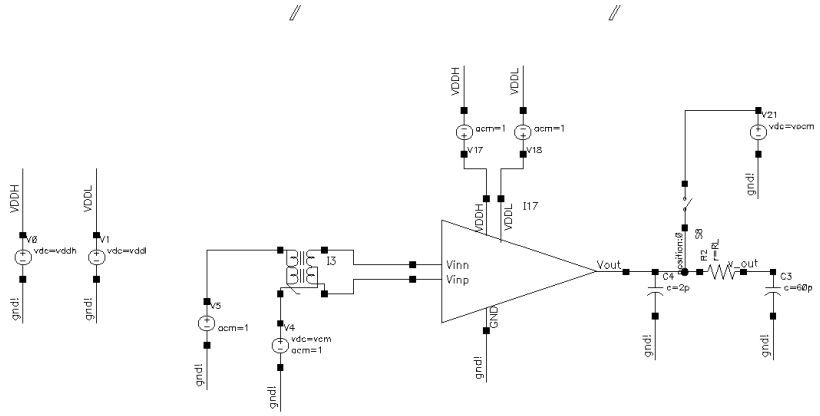


Figure 27: AC Test-Bench (Gain)

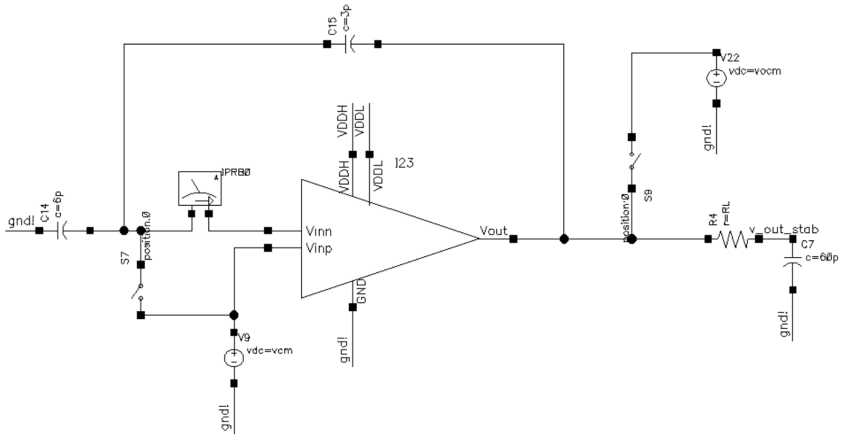


Figure 28: AC Test-Bench (Stability)

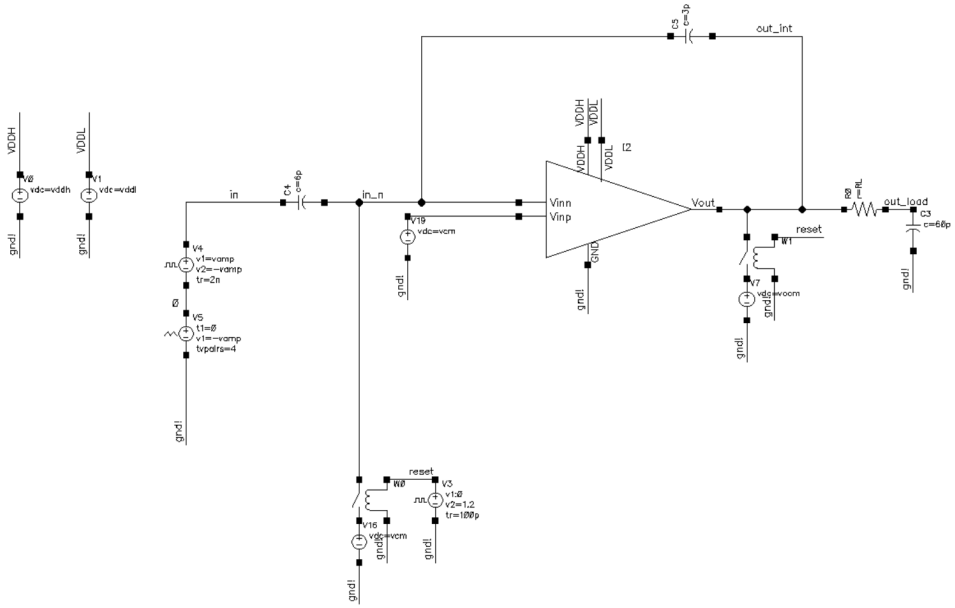


Figure 29: Transient Test-Bench

5 Conclusion

I designed a two-stage amplifier that successfully meets specifications while minimizing power. The amplifier has high enough open loop gain to have reliable closed loop gain, while high CMRR and PSRR maximize the signal-to-noise ratio. The amplifier has demonstrated ability to response to both small and large input steps, though with increasing mismatch as the input step grows.

My simulated results in Cadence matched my script-predicted values reasonably well throughout the design process, with my design requiring some iteration as expected due to approximations I intentionally made in my script, such as for the V_{DS} of each transistor.

Throughout the course of this project I have learned the necessary balance between arriving at a good starting point via scripts and understanding adjustments that will need to be made after simulation. I now better understand the complexities of biasing and how the ideal design must be biased such that it tracks process variations.

I understand that the source follower on my Class AB stage does not track process variations and attempted a monticelli design but was unable to successfully size it in time.

Overall, I am very grateful for this experience and look forward to further practicing analog design in future projects!